CLAIMS

What is claimed is:

1. A method of fabricating a vertical microelectromechanical device, the method comprising the steps of:

providing a bulk substrate;

selectively creating strong bond regions and weak bond regions on said substrate;

providing a first bonded semiconductor layer vertically supported on said substrate;

creating an electrode on said first bonded semiconductor layer, said electrodes corresponding to said weak bond regions;

creating an actuatable element disposed opposite said electrode;

removing said first semiconductor layer from said bulk substrate; and

bonding said first semiconductor layer to a second semiconductor layer.

2. The method of claim 1 further comprising the step of aligning said first semiconductor layer with said second semiconductor layer having similarly positioned electrodes.

3. The method of claim 2, wherein said aligning step is mechanical alignment.

4. The method of claim 2, wherein said aligning step is optical alignment.

5. The method of claim 1 further comprising the step of creating an electrode on said second semiconductor layer.

6. The method of claim 5, wherein said second semiconductor layer has semiconductor device portions on said weak bond regions.

7. The method of claim 1, wherein the ratio of areas of said strong bond regions to said weak bond regions is greater than 1.

8. The method of claim 1, wherein the ratio of bond strengths of said strong bond regions to said weak bond regions is greater than 1.

9. The method of clam 1 further comprising the step of interconnecting said first semiconductor layer with said second semiconductor layer.

10. The method of claim 9, wherein said step of interconnecting is implemented at the edge of said semiconductor layers.

11. The method of claim 10, wherein said step of interconnecting is electrically coupling.

12. The method of claim 10, wherein said step of interconnecting is optically coupling.

13. The method of claim 9, wherein said step of interconnecting is performed vertically through said semiconductor layers.

14. The method of claim 5, further comprising the steps of:

removing said second semiconductor layer from said bulk substrate; and

bonding said second semiconductor layer to said first semiconductor layer.

15. The method of claim 1, further comprising the steps of:

providing an Nth semiconductor layer vertically supported on said bulk substrate, said Nth semiconductor layer having strong bond regions and weak bond regions;

creating an electrode on said Nth semiconductor layer, said electrode corresponding to said weak bond regions;

removing said Nth semiconductor layer from said bulk substrate; and

bonding said Nth semiconductor layer to an (N-1)th semiconductor layer.

16. The method of claim 15, wherein MEMs devices are formed from any two of said N semiconductor layers.

17. The method of claim 1, further comprising the step of:

dicing said bonded semiconductor layers to form one or more dies.

18. The method of claim 17, further comprising the step of:

interconnecting said bonded semiconductor layers after said dicing step.

19. The method of claim 18, further comprising the step of:

forming edge connectors on the boundary of said one or more dies.

20. The method of claim 19 wherein said edge connectors serve as diagnostic conductors to determine health of individual die layers.

21. A vertical MEMs device comprising:

a bulk substrate on a wafer;

a first selectively bonded semiconductor layer vertically supported on said substrate, said bonded semiconductor layer containing weak bond regions and strong bond regions;

a second selectively bonded semiconductor layer vertically supported on said first selectively bonded semiconductor layer;

wherein an electrode and an actuatable element are created at or on said weak bond regions;

wherein said electrode and said actuatable element are disposed opposite each other, and

wherein said electrode and said actuatable element vertically spans said first selectively bonded semiconductor layer and said second selectively bonded semiconductor layer.

22. A vertical MEMs device formed on a die comprising:

a bulk substrate on a wafer;

a first selectively bonded semiconductor layer vertically supported on said substrate, said bonded semiconductor layer containing weak bond regions and strong bond regions;

a second selectively bonded semiconductor layer vertically supported on said first selectively bonded semiconductor layer;

wherein an element and an actuatable element are created at or on said weak bond regions;

wherein said element and said actuatable element vertically spans said first selectively bonded semiconductor layer and said second selectively bonded semiconductor layer, and

wherein said die is formed by dicing said bonded semiconductor layers.

23. The circuit of claim 22, wherein said die is rotated about its vertical axis to form a wiring stack.

24. The method of claim 1, wherein said bulk substrate includes a buried oxide layer.

25. The method of claim 24, wherein said buried oxide layer is formed by ion implantation.

26. A method of fabricating a multi layer microfluidic device, the method comprising the steps of:

providing a bulk substrate;

selectively creating strong bond regions and weak bond regions on said substrate;

providing a first bonded layer vertically supported on said substrate;

creating a port on said first bonded layer, said port corresponding to said weak bond regions;

creating a channel mechanically coupled to said port;

removing said first layer from said bulk substrate; and

bonding said first layer to a second layer.

27. The method of claim 26 further comprising the step of aligning said first layer with said second layer having similarly positioned ports.

28. The method of claim 27, wherein said aligning step is mechanical alignment.

29. The method of claim 27, wherein said aligning step is optical alignment.

30. The method of claim 26 further comprising the step of creating a port on said second layer.

31. The method of claim 30, wherein said second layer has microfluidic device portions on said weak bond regions.

32. The method of claim 26, wherein the ratio of areas of said strong bond regions to said weak bond regions is greater than 1.

33. The method of claim 26, wherein the ratio of bond strengths of said strong bond regions to said weak bond regions is greater than 1.

34. The method of clam 26 further comprising the step of interconnecting said first layer with said second layer.

35. The method of claim 34, wherein said step of interconnecting is implemented at the edge of said first and said second layers.

36. The method of claim 35, wherein said step of interconnecting is performed vertically through said first and said second layers.

37. The method of claim 34, further comprising the steps of:

removing said second layer from said bulk substrate; and

bonding said second layer to said first layer.

38. The method of claim 26, further comprising the steps of:

providing an Nth layer vertically supported on said bulk substrate, said Nth layer having strong bond regions and weak bond regions;

creating a port on said Nth layer, said port corresponding to said weak bond regions;

removing said Nth layer from said bulk substrate; and

bonding said Nth layer to an (N-1)th layer.

39. The method of claim 38, wherein microfluidic devices are formed from any two of said N layers.

40. The method of claim 26, further comprising the step of:

dicing said bonded layers to form one or more dies.

41. The method of claim 40, further comprising the step of:

interconnecting said bonded layers after said dicing step.

42. The method of claim 41, further comprising the step of:

forming edge connectors on the boundary of said one or more dies.

43. The method of claim 42 wherein said edge connectors serve as diagnostic indicators for determining the health of individual die layers.

44. The method of claim 26, wherein said bulk substrate includes a buried oxide layer.

45. The method of claim 44, wherein said buried oxide layer is formed by ion implantation.

46. A multilayer microfluidic device comprising:

a bulk substrate on a wafer;

a first selectively bonded layer vertically supported on said substrate, said bonded layer containing weak bond regions and strong bond regions;

a second selectively bonded layer vertically supported on said first selectively bonded layer;

wherein deconstructed ports and deconstructed channels are created at or on said weak bond regions, and

wherein said ports and channels vertically span said first selectively bonded layer and said second selectively bonded layer.

47. A multilayer microfluidic device formed on a die comprising:

a bulk substrate on a wafer;

a first selectively bonded layer vertically supported on said substrate, said bonded layer containing weak bond regions and strong bond regions;

a second selectively bonded layer vertically supported on said first selectively bonded layer;

wherein deconstructed ports and deconstructed channels are created at or on said weak bond regions;

wherein said ports and channels vertically span said first selectively bonded layer and said second selectively bonded layer, and

wherein said die is formed by dicing said bonded semiconductor layers.

48. The circuit of claim 47, wherein said die is rotated about its vertical axis to form a stack.